UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,898,648 B2
APPLICATION NO. : 10/081652
DATED : May 24, 2005
INVENTOR(S) : Paul A. LaBerge

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column, Line	Reads	Should Read
Item (54)	"MEMORY BUS POLARITY INDICATOR SYSTEM AND METHOD FOR REDUCING THE AFFECTS OF SIMULTANEOUS SWITCHING OUTPUTS (SSO) ON MEMORY BUS TIMING"	--MEMORY BUS POLARITY INDICATOR SYSTEM AND METHOD FOR REDUCING THE EFFECTS OF SIMULTANEOUS SWITCHING OUTPUTS (SSO) ON MEMORY BUS TIMING--
Item (57), Line 7	"data contained each"	--data contained in each--
Column 1, Line 3	"THE AFFECTS OF"	--THE EFFECTS OF--
Column 1, Line 16	"system are clock""	--system are--
Column 2, Line 8	"in response rising"	--in response to rising--
Column 2, Line 36	"modem synchronous"	--modern synchronous--
Column 3, Lines 11-12	"thereby undesirable shifts"	--thereby undesirably shifts--
Column 4, Line 39	"of bits the data words"	--of bits of the data words--
Column 4, Line 51	"contained each read data"	--contained in each read data--
Column 7, Line 14	"data bus DATA bus"	--data bus DATA--
Column 8, Line 54	"that in the memory"	--that the memory--
Column 8, Line 62	"would typically includes"	--would typically include--
Column 9, Line 16	"for the inverted next"	--or the inverted next--

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 6,898,648 B2
APPLICATION NO. : 10/081652
DATED : May 24, 2005
INVENTOR(S) : Paul A. LaBerge

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 9, Line 26	"is coupled to tell with"	--is coupled with--
Column 9, Line 32	"either the NDW<1:N> for"	--either the NDW<1:N> or--
Column 9, Line 67	"determines number of bits"	--determines the number of bits--
Column 10, Line 12-13	"determines number of bits"	--determines the number of bits--
Column 11, Line 6	"inverted DL-DM words"	--inverted D1-DM words--
Column 11, Line 52	"data bus inversion word"	--data bus inversion words--
Column 11, Line 56	"an segment"	--a segment--
Column 11, Line 66	"inversion bit I1 bit is cleared"	--inversion bit I1 is cleared--
Column 12, Line 17	"for an extra dedicated"	--for extra dedicated--
Column 12, Line 38	"there are 8 data word"	--there are 8 data words--
Column 12, Line 46	"in the DBI<1:*> may need"	--in the DBI<1:8> word may need--
Column 13, Line 47	"such as output"	--such output--
Column 14, Line 23	"word, and"	--word; and--
Column 14, Lines 29-30	"on an associated data masking pins."	--on an associated data masking pin.--
Column 14, Line 37	"plurality of data masking pin"	--plurality of data masking pins--

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

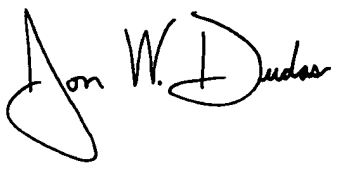
PATENT NO. : 6,898,648 B2
APPLICATION NO. : 10/081652
DATED : May 24, 2005
INVENTOR(S) : Paul A. LaBerge

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 15, Line 44	"and apply an active a data"	--and apply an active data--
Column 16, Line 10	"to a clocks signal; and"	--to a clock signal; and--
Column 16, Line 40	"received write data words invert or not invert"	--received write data words to invert or not invert--
Column 16, Line 51	"word including the data bus inversion data applies to a"	--word, including the data bus inversion data, applies to a--
Column 17, Line 48	"to a clocks signal; and"	--to a clock signal; and--
Column 18, Line 34	"received write data words invert or not invert"	--received write data words to invert or not invert--

Signed and Sealed this

First Day of January, 2008



JON W. DUDAS
Director of the United States Patent and Trademark Office